(12) UK Patent Application (19) GB (11) 2 161 649 A

(43) Application published 15 Jan 1986

(21) Application No 8513599

(22) Date of filing 30 May 1985

(30) Priority data

(31) 59/110244 (32) 30 May 1984 (33) JP
59/204427 29 Sep 1984
59/244811 20 Nov 1984

(51) INT CL[4]
H01L 29/08 29/68

(52) Domestic classification
H1K 1AA9 1AB9 1CA 4C11 4C14 4C2B 4C2U 4H1A 4H3A 9B3 9B4X 9D1 9E 9N2 9N3 9P1 9P2 9R2 AAX CAX

(56) Documents cited
GB A 2088631

(58) Field of search
H1K

(71) Applicants
Kabushiki Kaisha Toshiba (Japan)
72 Horikawa-cho, Saiwai-ku, Kawasaki-shi, Japan

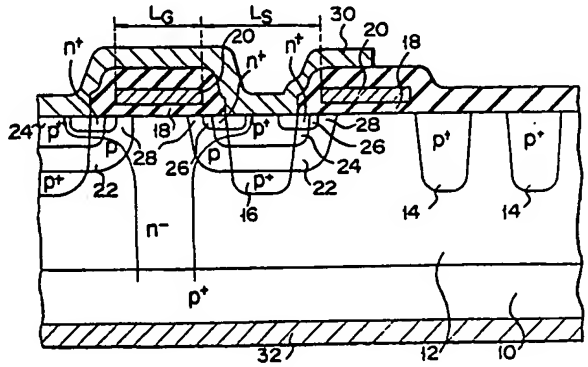
(72) Inventors
Akio Nakagawa
Hiromichi Ohashi
Yoshihiro Yamaguchi
Kiminori Watanabe
Thuneo Thukakoshi

(74) Agent and/or Address for Service
Marks and Clerk, 57-60 Lincoln's Inn Fields, London WC2A 3LS

(54) Conductivity modulated MOSFET

(57) A conductivity modulated MOSFET, having a semiconductor substrate (10) of a first conductivity type, a semiconductor layer (12) of a second conductivity type formed on the semiconductor substrate and having a high resistance, a base layer (22) of the first conductivity type formed in the semiconductor layer, a source layer (26) of the second conductivity type formed in the base layer, a gate electrode (20) formed on a gate insulating film (18) which is formed on a channel region, the channel region being formed in a surface of the base layer between the semiconductor layer and the source layer, a source electrode (30) ohmic-contacting the source layer and the base layer, and a drain electrode (32) formed on the surface of the semiconductor substrate opposite to the semiconductor layer, characterized in that the conductivity modulated MOSFET has a saturation current smaller than a latch-up current when a predetermined gate voltage is applied to the gate electrode. Alternatively the drain electrode may be formed on the same surface as the source electrode to provide a lateral MOSFET.

F I G. 2



GB 2 161 649 A

FIG. 1

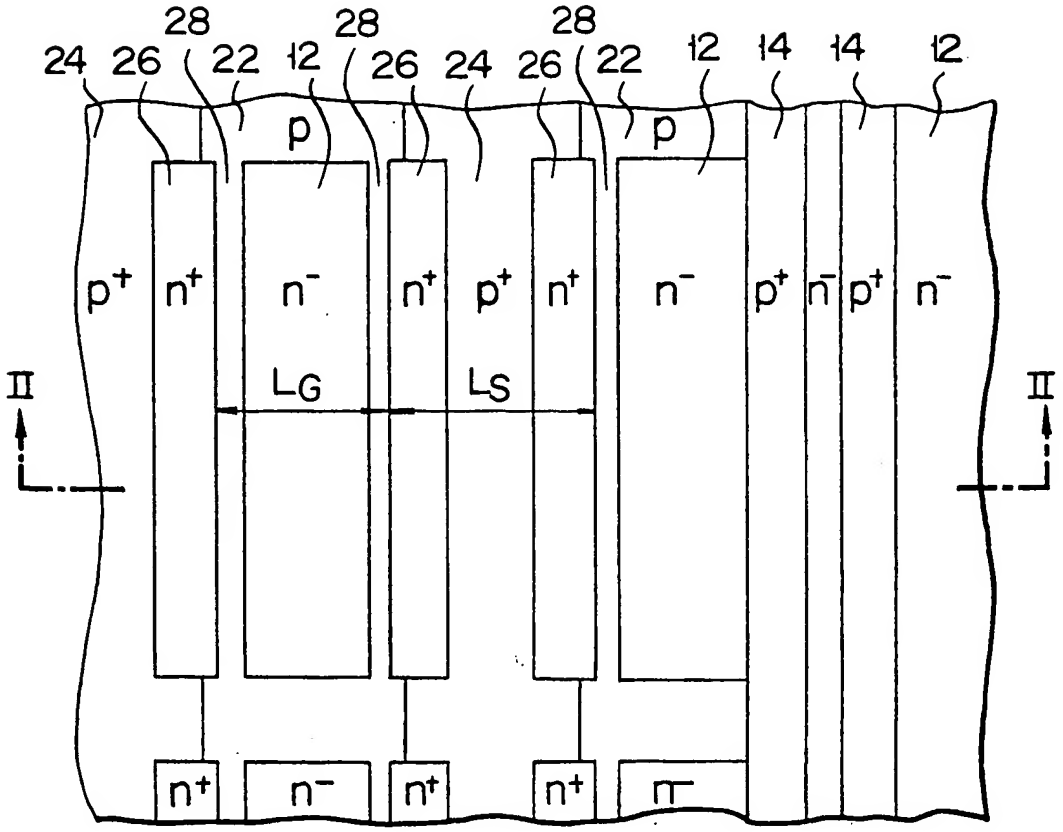

28
28
28
24
26
22
12
26
24
26
22
12
14
14
12
p
p
p+
n+
n−
n+
p+
n+
n−
p+
n−
p+
n−
II
LG
LS
II
n+
n−
n+
n+
n−

FIG. 2

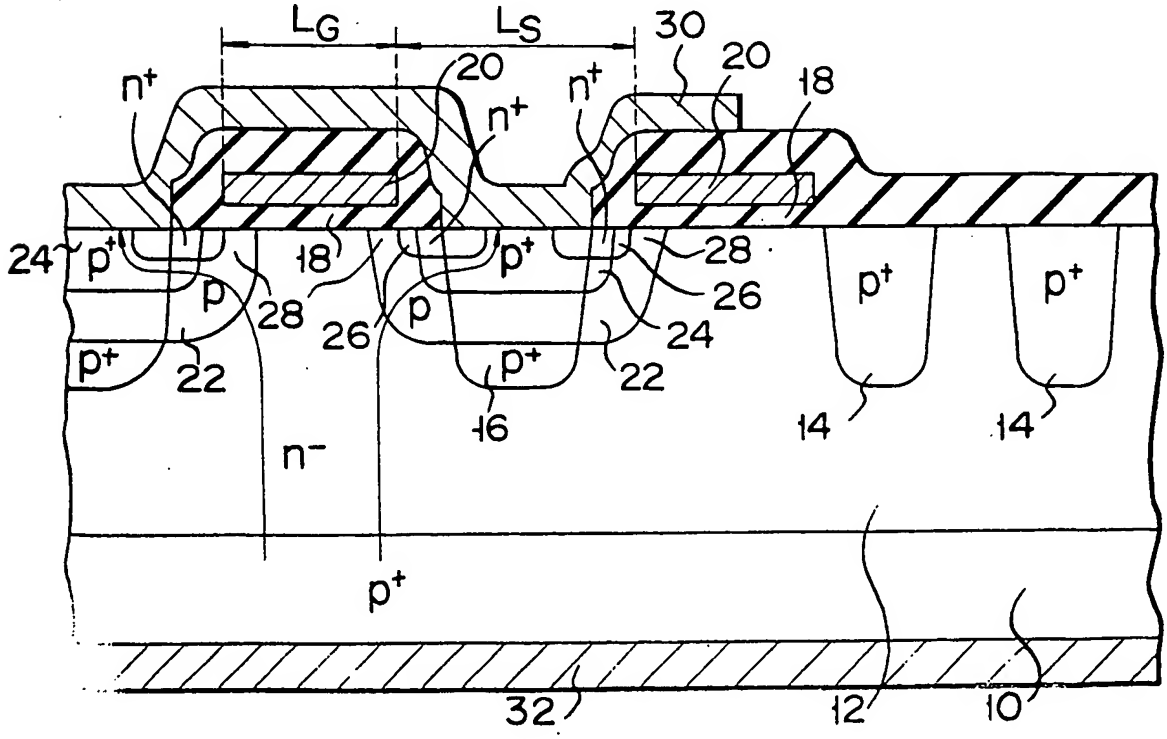

LG
LS
30
20
20
18
n+
n+
n+
24
p+
18
p+
28
p+
p+
p
p
p
28
26
26
24
p+
22
p+
22
16
14
14
n−
p+
32
12
10

FIG. 3

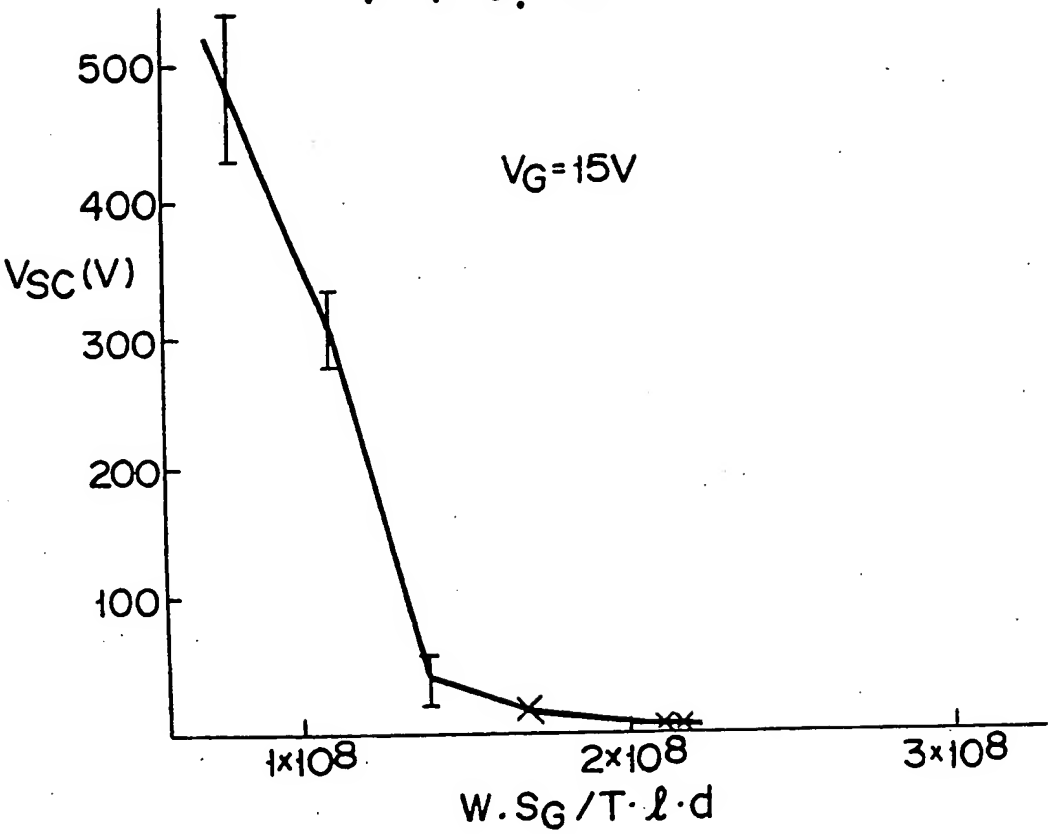

500
400
300
200
100
VSC(V)
VG=15V
1x10^8
2x10^8
3x10^8
W.SG/T·ℓ·d

FIG. 4

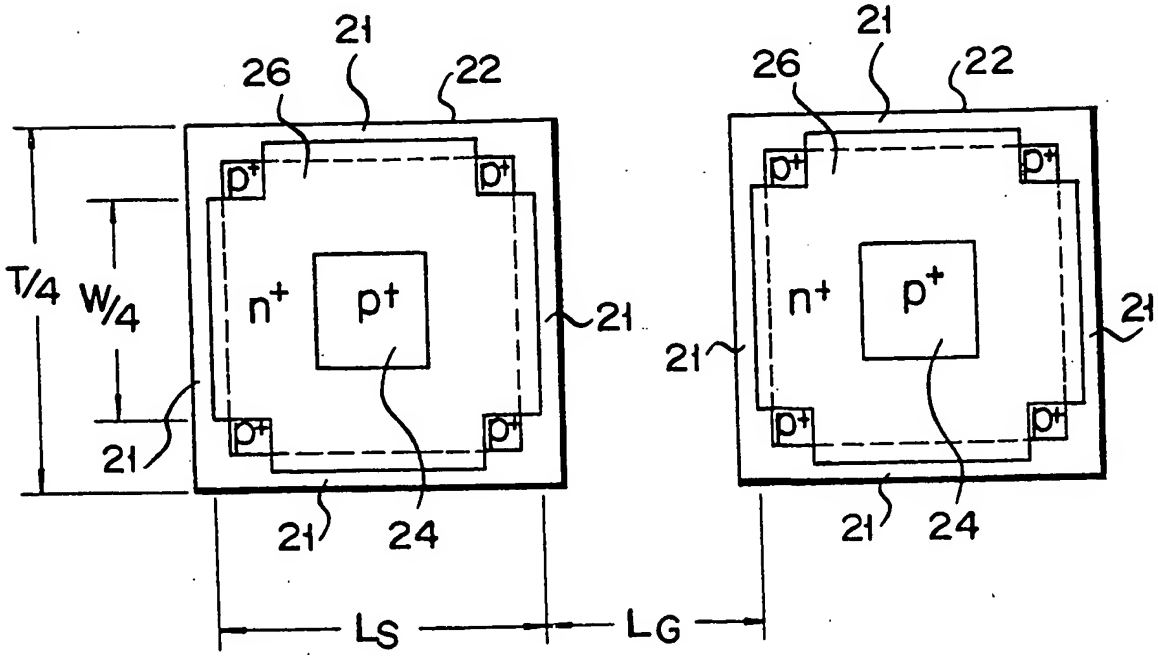

21
26
22
p+
n+
T/4
W/4
24
LS
LG

FIG. 5

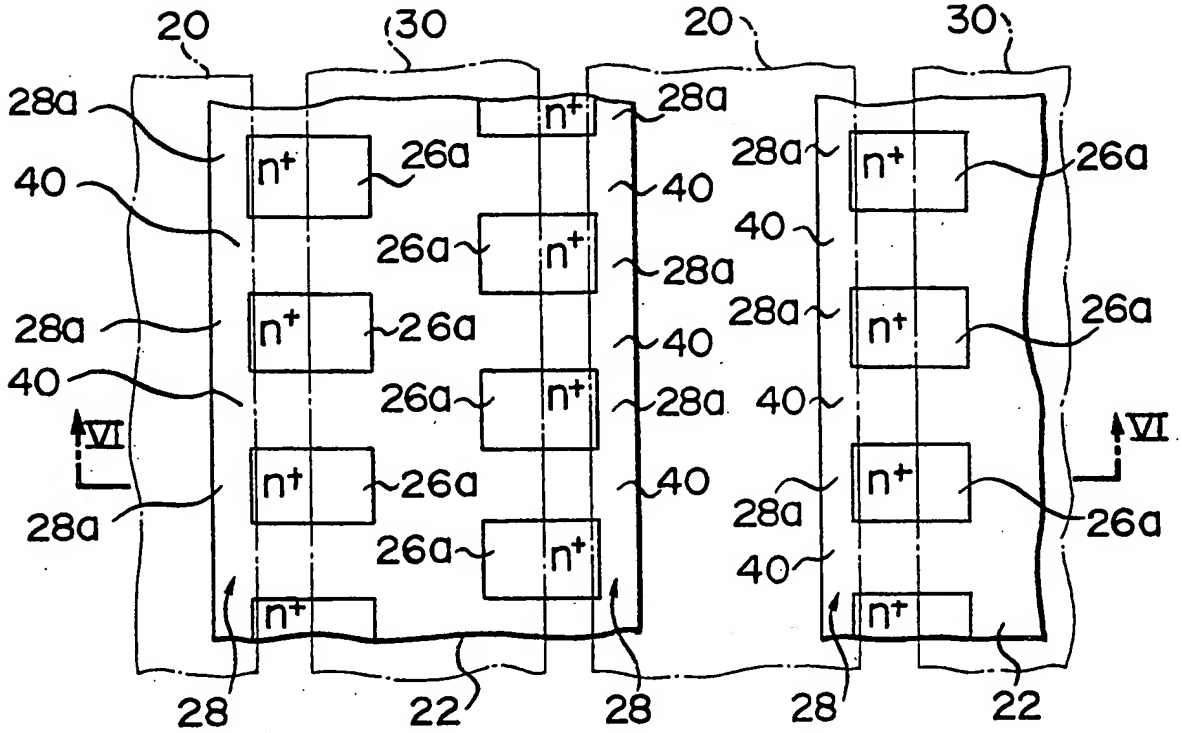

20
30
20
30
28a
40
n+
26a
VI
28
22

FIG. 6

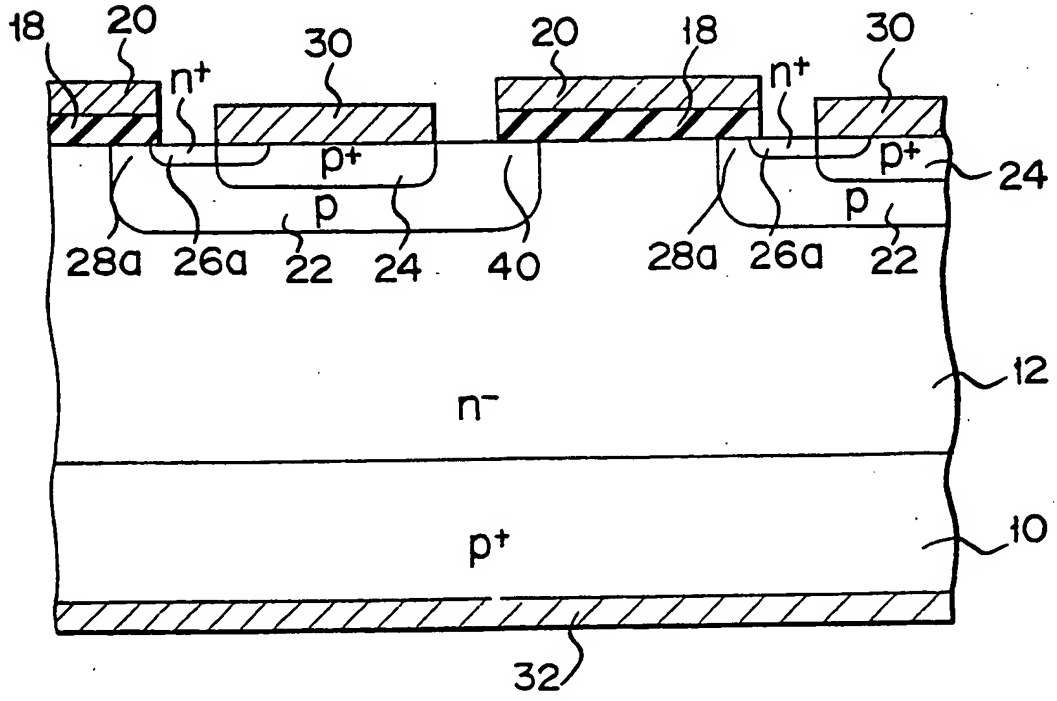

18
20
30
n+
p+
p
28a
26a
22
24
40
n−
12
p+
10
32

FIG. 7

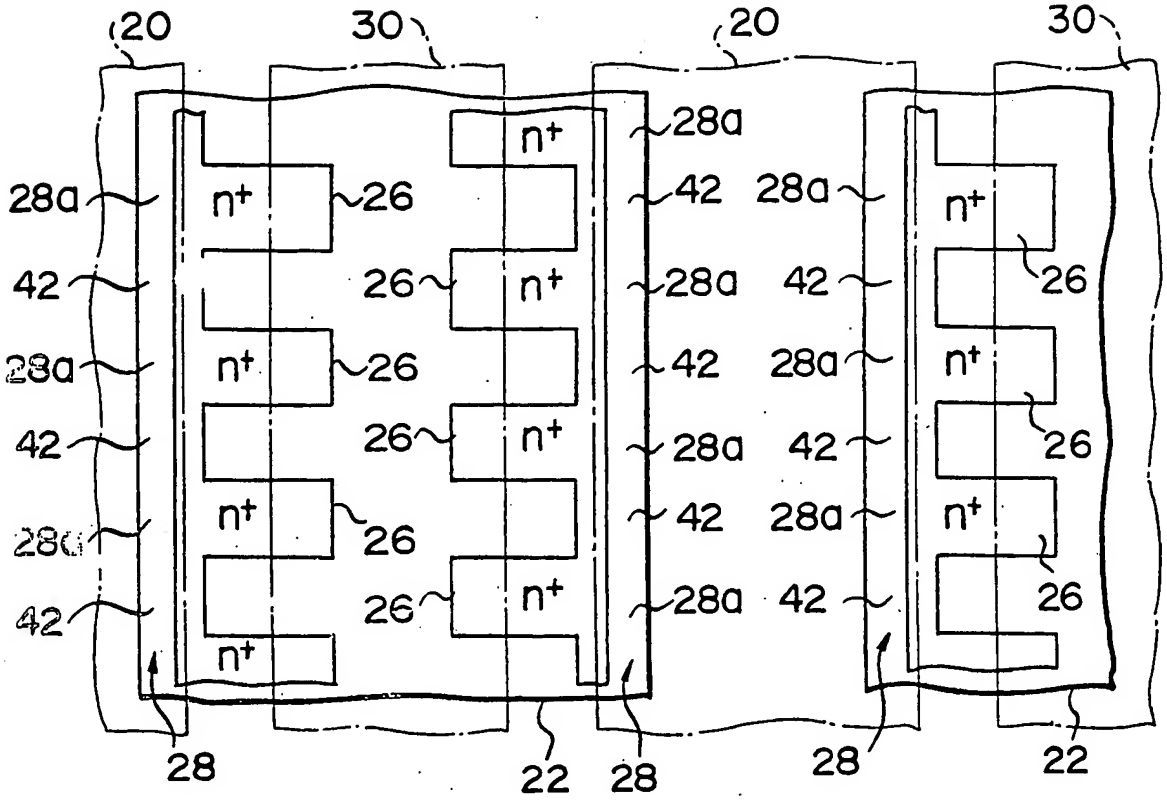

20
30
20
30
28a
42
28a
42
28a
42
28a
42
n+
26
28a
42
28a
42
28a
42
28a
42
28
22
28
28
22

FIG. 8

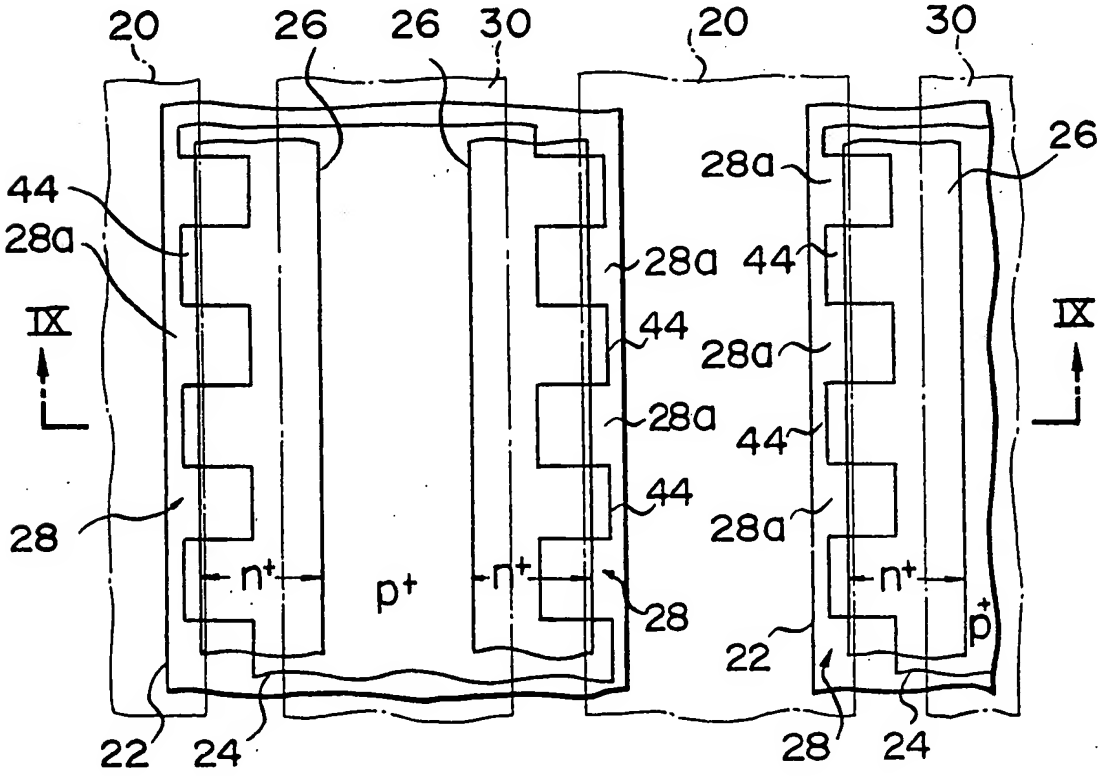

20
26
26
30
20
30
44
28a
IX
28
n+
p+
n+
28
22
24
28a
44
28a
44
28a
44
28a
44
28a
26
IX
n+
p+
22
28
24

FIG. 9

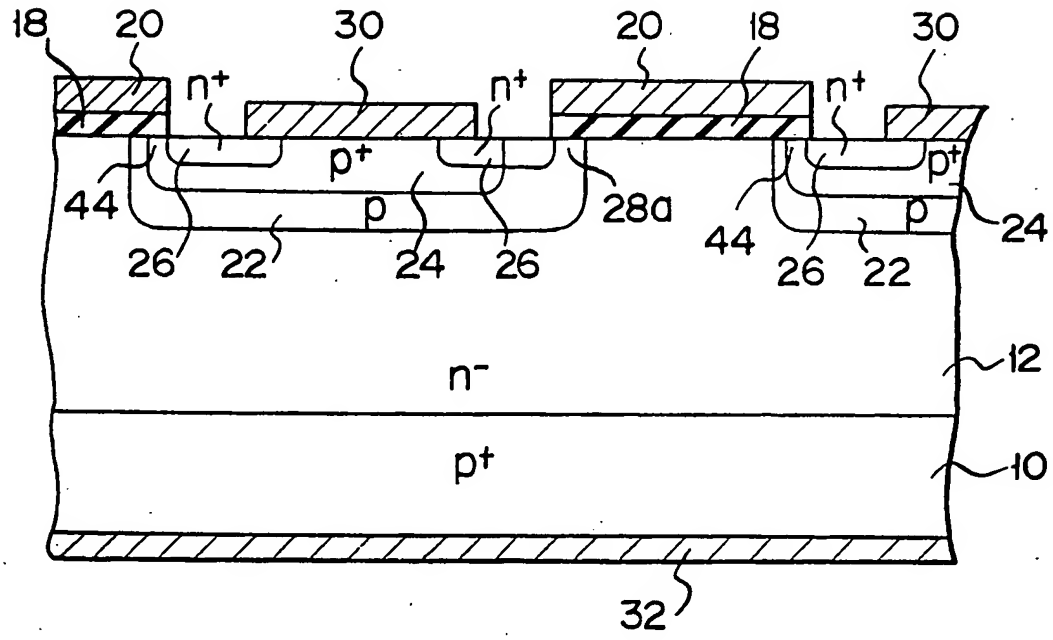

18
20
30
20
18
30
n+
n+
n+
p+
p+
44
p
p
28a
44
24
26
22
24
26
26
22
n-
12
p+
10
32

FIG. 10

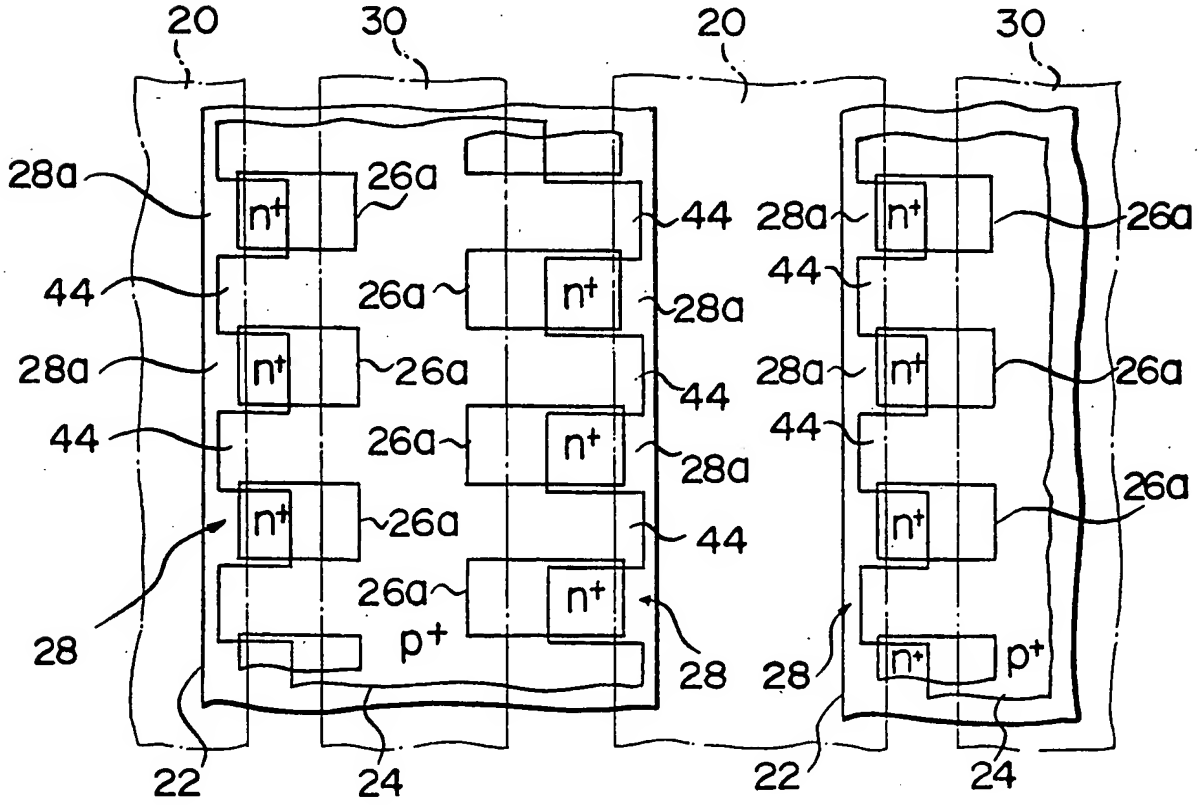

20
30
20
30
28a
26a
n+
44
28a
n+
26a
44
26a
n+
28a
44
28a
n+
26a
28a
n+
26a
44
44
26a
n+
28a
44
n+
26a
44
26a
n+
26a
n+
28
p+
28
28
n+
p+
22
24
22
24

FIG. 11

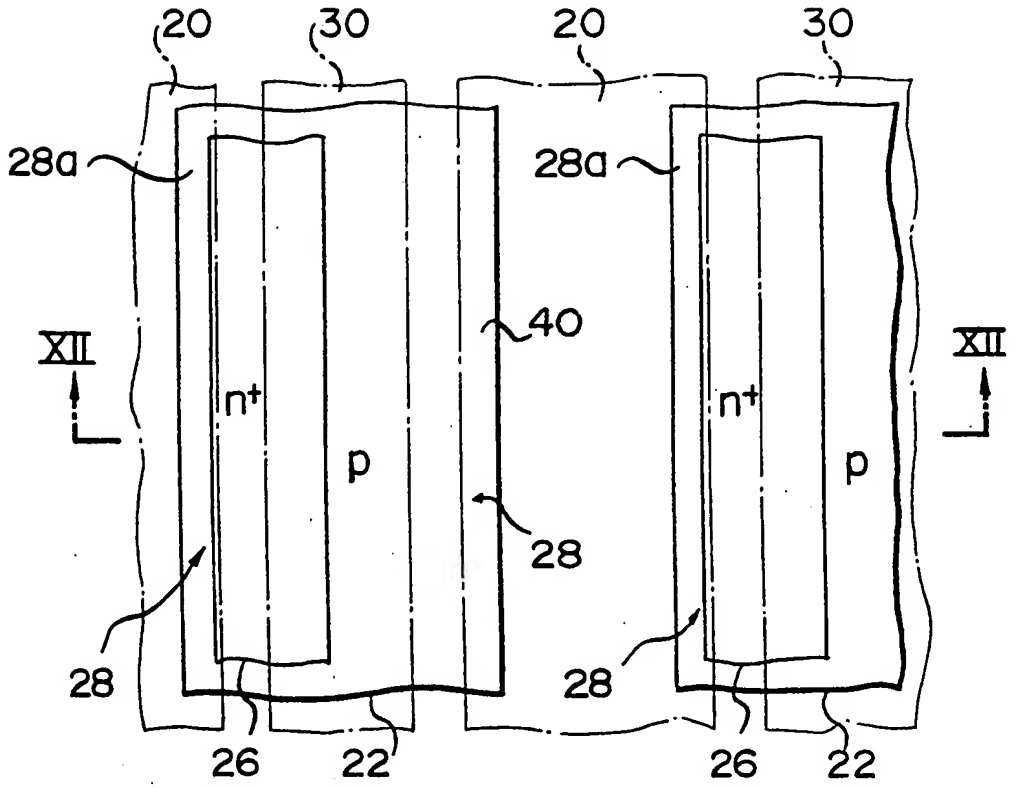

20
30
20
30
28a
28a
XII
XII
40
n+
p
n+
p
28
28
28
26
22
26
22

FIG. 12

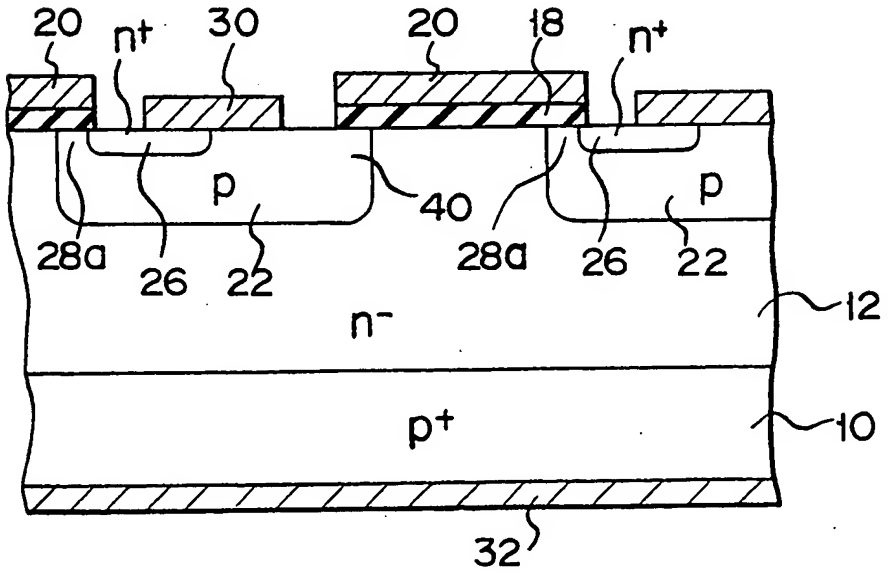

20
n+
30
20
18
n+
p
p
40
28a
28a
26
22
26
22
n-
12
p+
10
32

FIG. 13

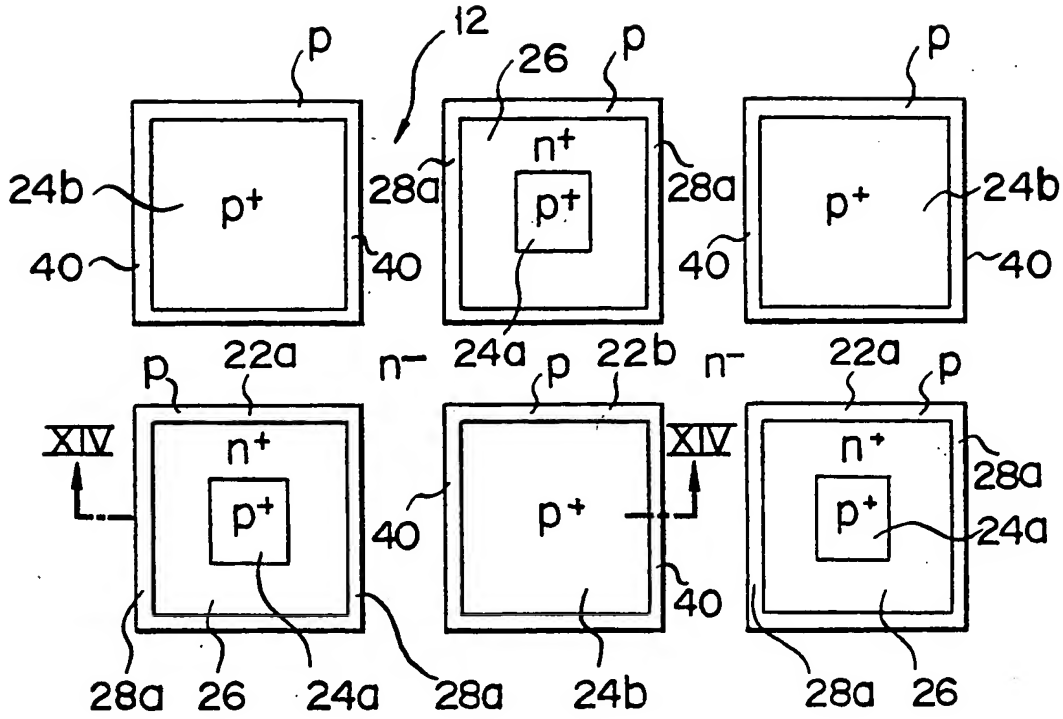

p
12
26
p
p
24b
p+
28a
n+
p+
28a
p+
24b
40
40
40
40
22a
n−
24a
p
22b
n−
22a
p
XIV
n+
p+
40
p+
XIV
n+
p+
28a
24a
28a
26
24a
28a
24b
28a
26

FIG. 14

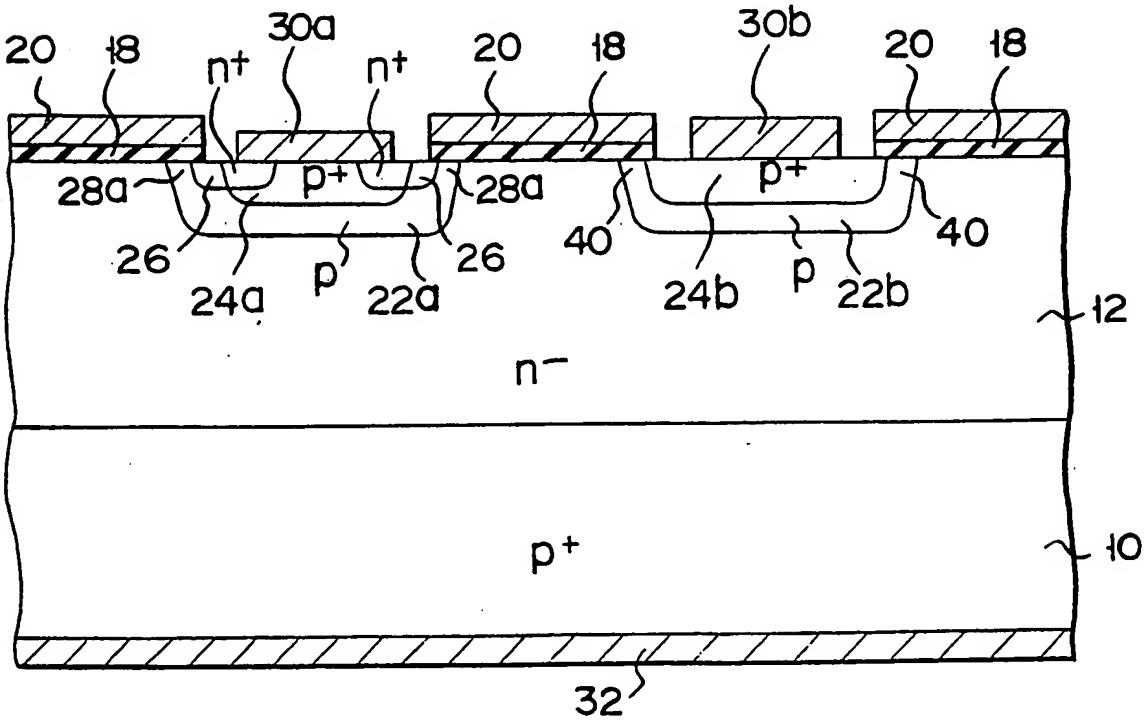

20
18
30a
n+
n+
20
18
30b
20
18
28a
p+
28a
p+
26
24a
p
22a
26
40
24b
p
22b
40
12
n−
p+
10
32

FIG. 15

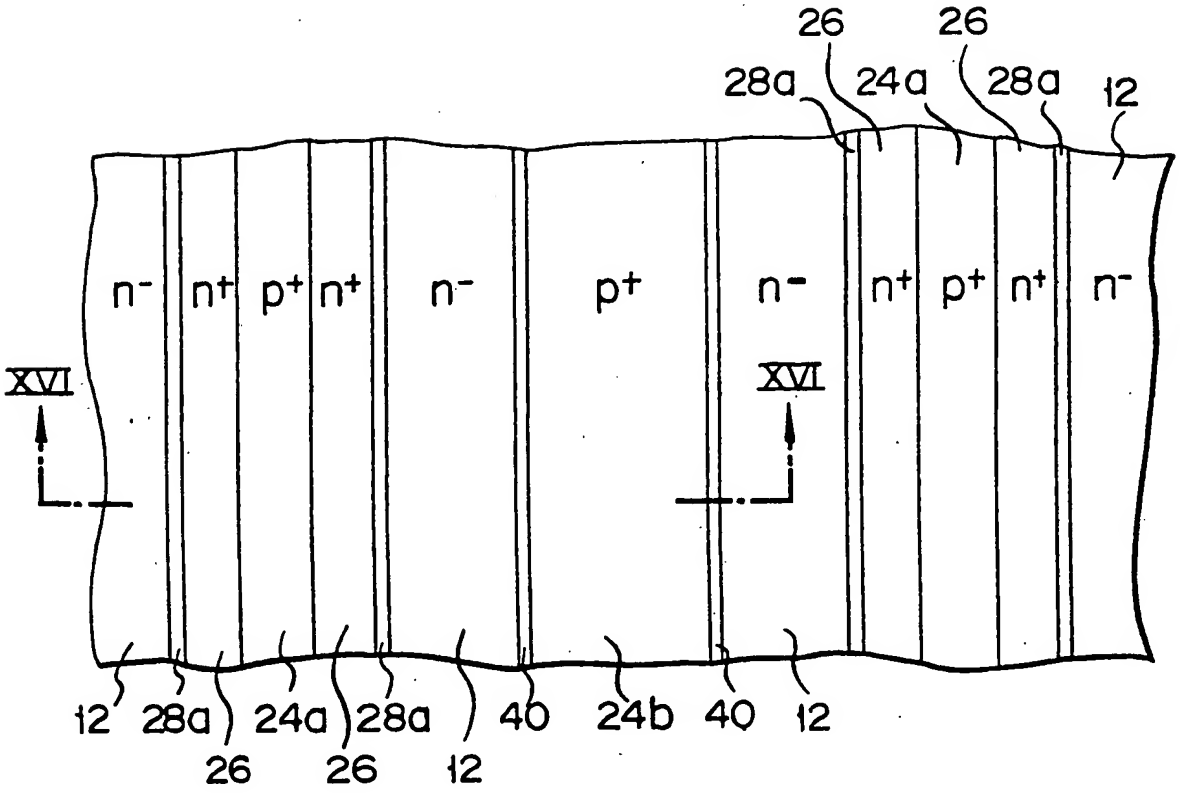

26
26
28a
24a
28a
12
n⁻
n⁺
p⁺
n⁺
n⁻
p⁺
n⁻
n⁺
p⁺
n⁺
n⁻
XVI
XVI
12
28a
24a
28a
40
24b
40
12
26
26
12

FIG. 16

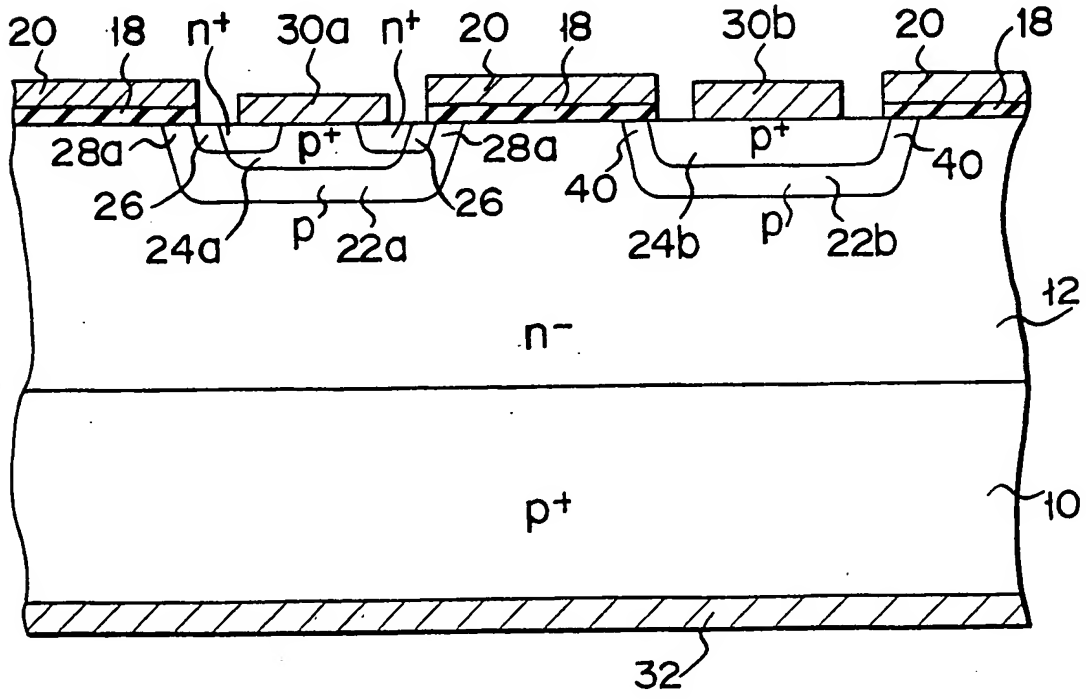

20
18
n⁺
30a
n⁺
20
18
30b
20
18
28a
p⁺
28a
p⁺
40
40
26
26
24a
p
22a
40
24b
p
22b
12
n⁻
p⁺
10
32

FIG. 17

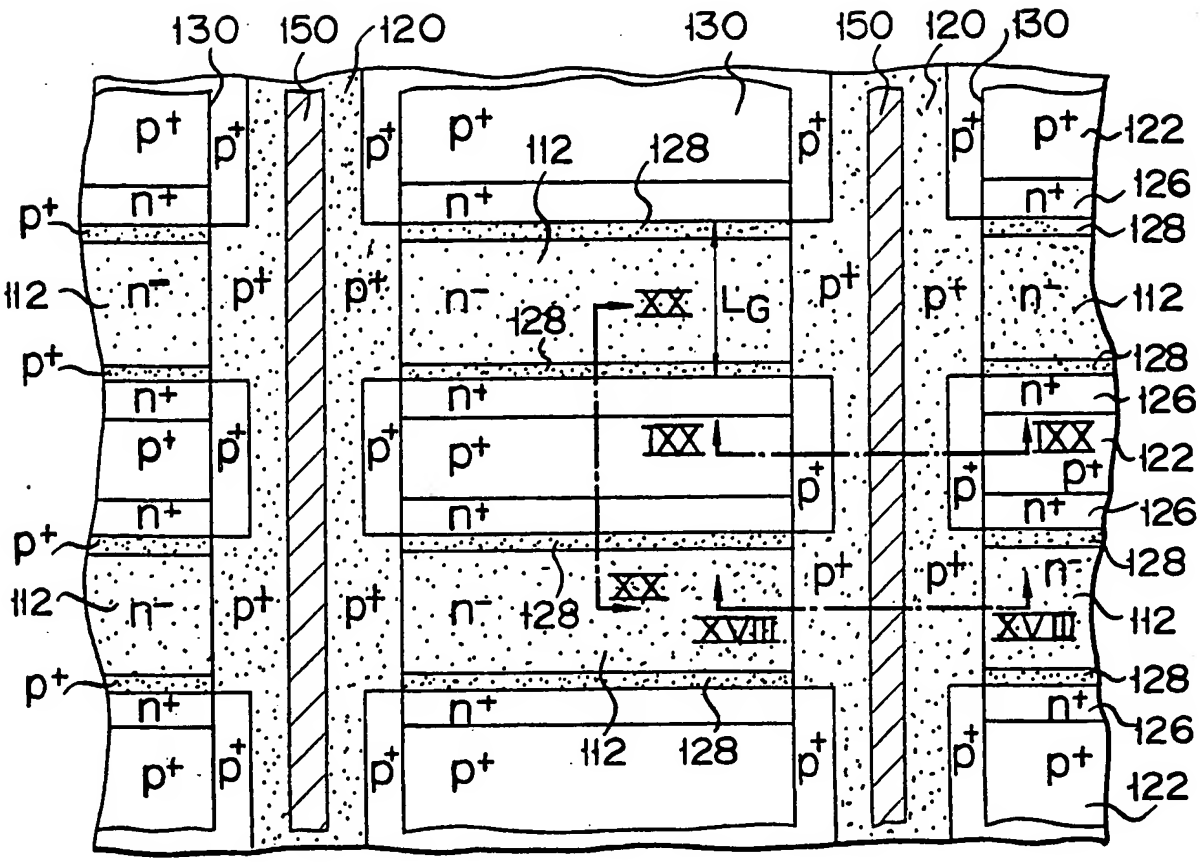

130
150
120
130
150
120
130
p+
n+
n−
112
128
122
126
XX
XXX
XVIII
LG

FIG. 18

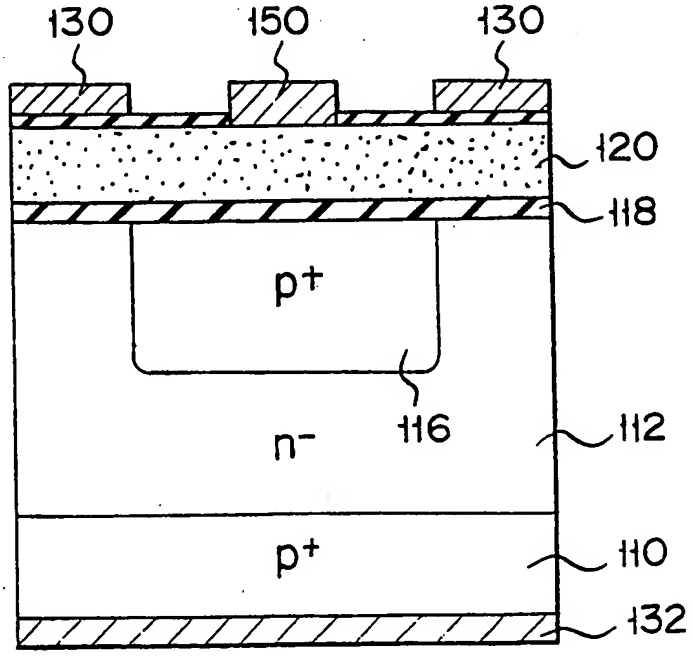

130
150
130
120
118
p+
116
112
n−
p+
110
132

FIG. 19

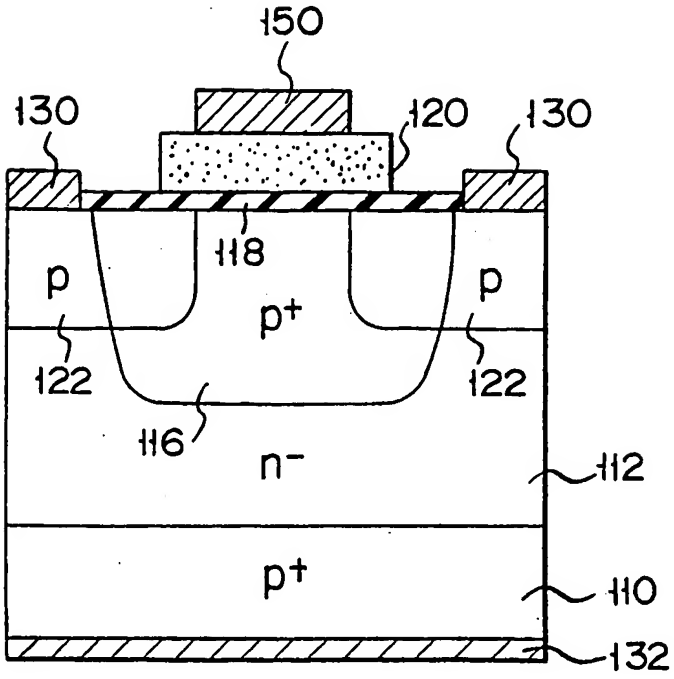

150
130
120
130
118
p
p+
p
122
122
116
n-
112
p+
110
132

FIG. 20

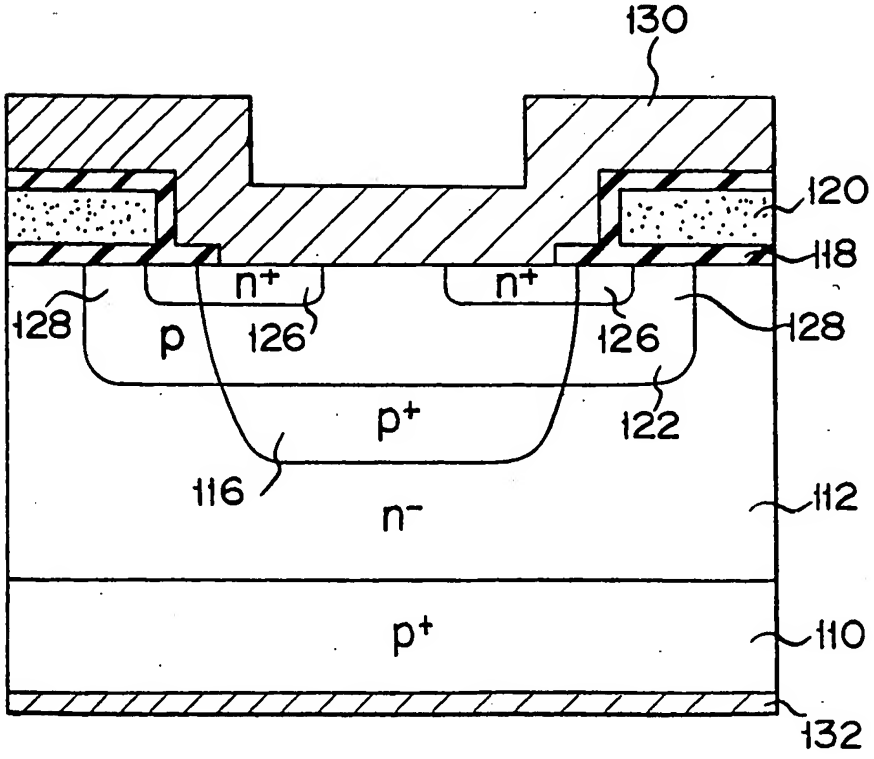

130
120
118
n+
n+
128
p
126
126
128
p+
122
116
n-
112
p+
110
132

FIG. 21

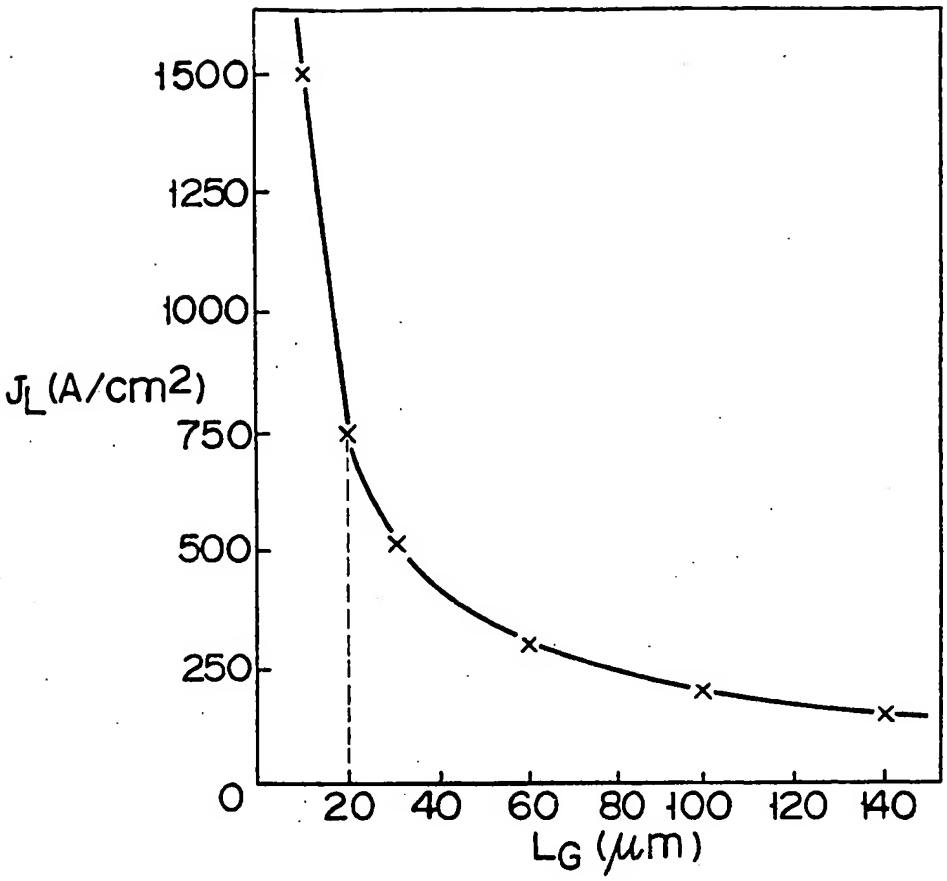

1500
1250
1000
750
500
250
0
J_L (A/cm2)
20
40
60
80
100
120
140
L_G (μm)

FIG. 22

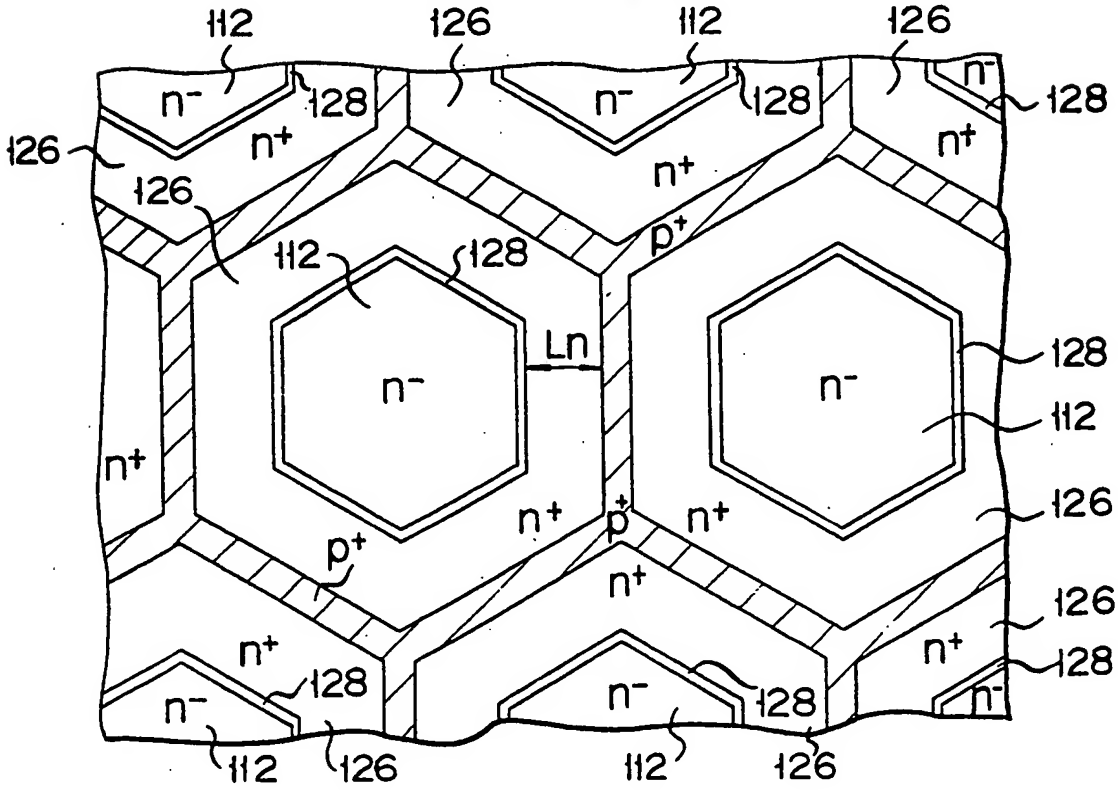

112
126
n⁻
128
n⁺
p⁺
Ln

FIG. 23

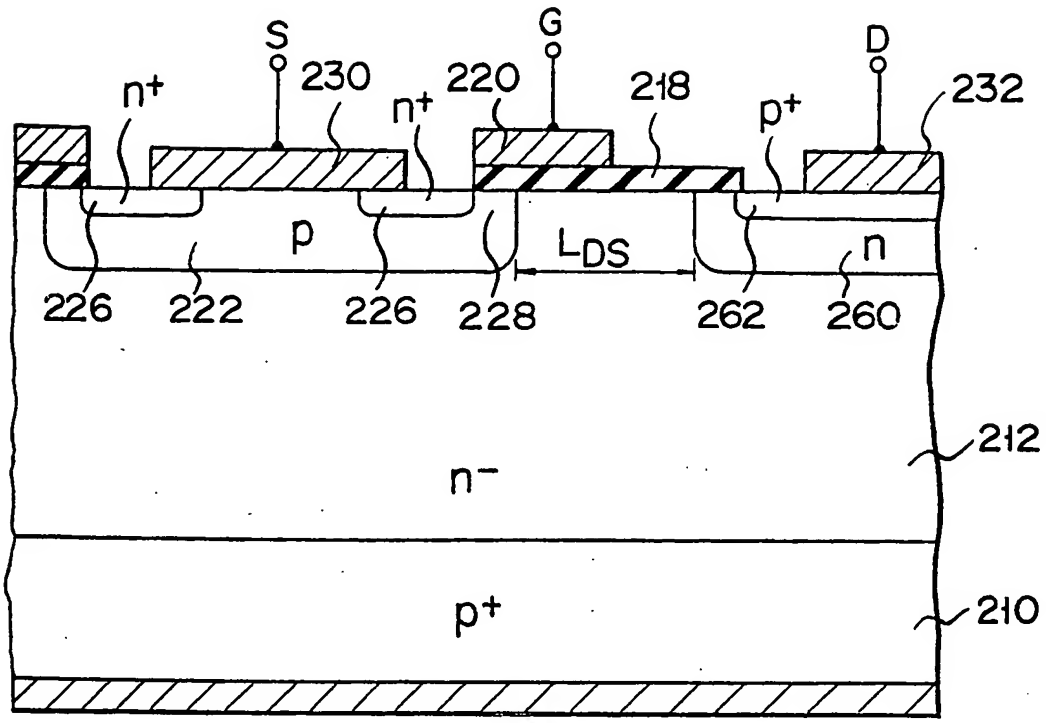
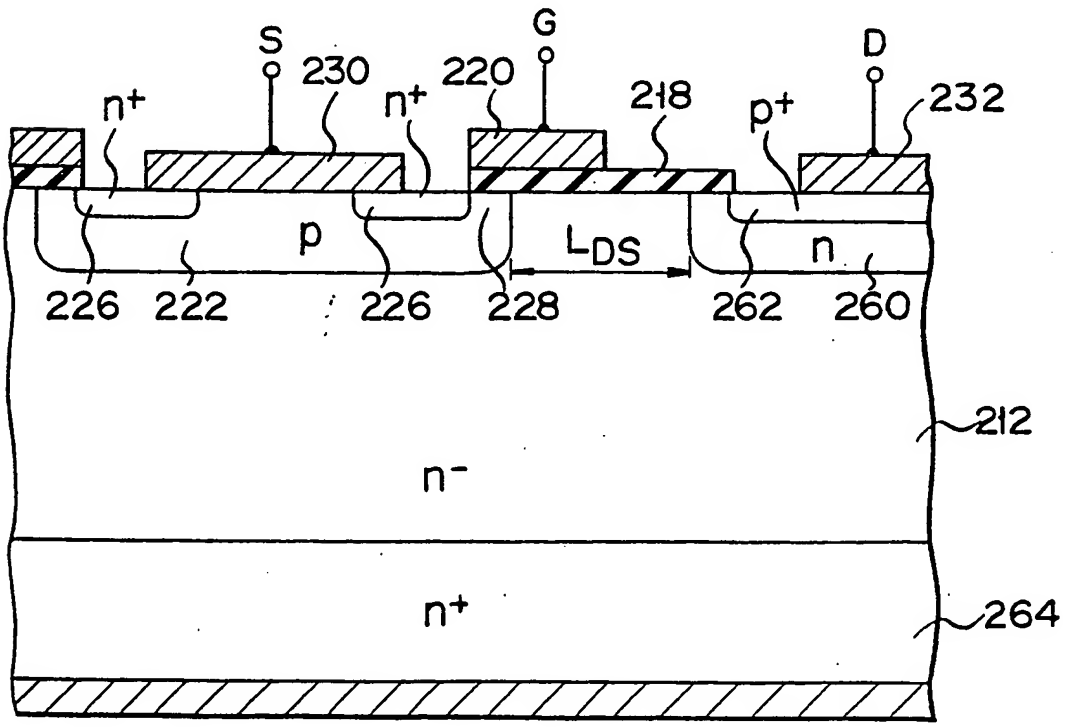

S
G
D
n+
230
n+
220
218
p+
232
p
LDS
n
226
222
226
228
262
260
212
n−
p+
210

FIG. 24


S
G
D
n+
230
n+
220
218
p+
232
p
LDS
n
226
222
226
228
262
260
212
n−
n+
264

SPECIFICATION

Conductivity modulated MOSFET

The present invention relates to a conductivity modulated MOSFET.

A conductivity modulated MOSFET has a drain region whose conductivity type is opposite to that of a source region of a normal power MOSFET. Typical examples of conventional conductivity modulated MOSFETs are described by M.F. Chang et al., "25 AMP, 500 Volt Insulated Gate Transistors", 1983 IEEE IEDM Technical Digest PP. 83 - 86 and by A.M. Goodman et al., "Improved COMFETs with Fast Switching Speed and High-current Capability", 1983 IEEE IEDM Technical Digest PP. 79 - 82.

Such a conductivity modulated MOSFET has a parasitic p-n-p-n thyristor. When the parasitic thyristor is turned on, the MOSFET cannot be turned off even if a voltage across the gate and source thereof is zero. The element is often damaged. The parasitic thyristor is turned on since holes injected from the p^+-type drain layer into an n^--type drain region pass into the source electrode through a p-type base layer. In other words, when a hole current flows through the p-type base layer and voltage drop across a resistor of the base layer immediately under the source layer exceeds 0.7 V, electrons are injected from the source layer to turn on the parasitic thyristor. This phenomenon is described in the above-mentioned "25 AMP, 500 Volt Insulated Gate Transistors".

In order to prevent such a latch-up phenomenon, various proposals have been made including the two papers described above. The present invention, however, has been made to prevent the latch-up phenomenon from another viewpoint.

It is an object of the present invention to provide a conductivity modulated MOSFET which prevents a latch-up phenomenon caused by a parasitic thyristor.

In order to achieve the above object of the present invention, there is provided a conductivity modulated MOSFET, comprising: a semiconductor substrate of a first conductivity type which has first and second surfaces; a high resistance semiconductor layer of a second conductivity type which is formed on the first surface of the semiconductor substrate and has a high resistance, the high resistance semiconductor layer being provided with a third surface contacting the first surface and a fourth surface opposite to the third surface; a base layer of the first conductivity type which is formed in the fourth surface of the high resistance semiconductor layer; a source layer of the second conductivity type which is formed by diffusion in the base layer; a gate electrode formed on a gate insulating film which is formed on a channel region, the channel region being formed in a surface of the base layer between the fourth surface of the high resistance semiconductor layer and the source layer; a source electrode ohmic-contacting the source layer and the base layer; and a drain electrode formed on the second surface of the semiconductor substrate, characterized in that the conductivity modulated MOSFET has a saturation current smaller than a latch-up current when a predetermined gate voltage is applied to the gate electrode.

With the above arrangement, the current flowing through the conductivity modulated MOSFET is always smaller than the latch-up current, thereby preventing the latch-up phenomenon in principle.

There are several methods for setting the saturation current of the conductivity modulated MOSFET to be smaller than the latch-up current. The following methods are included therein as will be described in detail with reference to the preferred embodiments.

(1) To satisfy $(W \cdot SG)/(T \cdot l \cdot d) < 1.46 \times 10^8$ where
W: an overall channel width (μm) per unit area (113^2) of an effective element region
SG: an area (μm^2) of a portion of the gate electrode which is formed immediately on the high resistance semiconductor layer within the unit area
T: an overall circumferential length (μm) of the base layer within the unit area
l: a channel length (μm) and
d: a thickness (μm) of the gate insulating film.

(2) To satisfy $(W \cdot SG)/(T \cdot l \cdot d) < 1.1 \times 10^8$ where
W: the overall channel width (μm) per unit area (1 cm^2) of an effective element region
SG: an area (μm^2) of a portion of the gate electrode which is formed immediately on the high resistance semiconductor layer within the unit area
T: an overall circumferential length (μm) of the base layer within the unit area
l: a channel length (μm) and
d: a thickness (μm) of the gate insulating film.

(3) To form portions which are not or can hardly be subjected to MOSFET operation between the source electrode and the fourth surface of the high resistance semiconductor layer. The portions which are not subjected to MOSFET operation are formed as portions without the source layer along the direction of the channel width, thereby forming a hole current path from the drain to the source electrode without being through a portion under the source layer.

(4) To surround the fourth surface of the high resistance semiconductor layer by the base layer to constitute an island region.

Other objects and advantages will be apparent from the following description taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a plan view of a conductivity modulated MOSFET according to a first embodiment of the present invention;

Fig. 2 is a sectional view of the MOSFET taken along the line II - II of Fig. 1;

Fig. 3 is a graph showing a relationship between VSC (a voltage applied to an element) and $W \cdot SG/T \cdot l \cdot d$ (A 50 Ω resistor was inserted between the gate terminal and the gate circuit), where W is an overall channel width (μm) per unit area (1 cm^2) in an effective element region, SG is an area (μm^2) of a portion of the gate electrode which is formed immediately on the high resistance semiconductor layer within the unit area, T is an overall circumferential length (μm) of the base layer within the unit area, l is a channel length (μm) and d is a thickness (μm) of the gate insulating film;

Fig. 4 is a plan view of a conductivity modulated MOSFET according to a second embodiment of the present invention;

Fig. 5 is a plan view of a conductivity modulated

MOSFET according to a third embodiment of the present invention;

Fig. 6 is a sectional view of the MOSFET taken along the line VI - VI of Fig. 5;

Fig. 7 is a plan view showing a modification of the conductivity modulated MOSFET shown in Fig. 5;

Fig. 8 is a plan view of a conductivity modulated MOSFET according to a fourth embodiment of the present invention;

Fig. 9 is a sectional view of the MOSFET taken along the line IX - IX of Fig. 8;

Fig. 10 is a plan view showing a modification of the conductivity modulated MOSFET of Fig. 8;

Fig. 11 is a plan view of a conductivity modulated MOSFET according to a fifth embodiment of the present invention;

Fig. 12 is a sectional view of the MOSFET taken along the line XII - XII of Fig. 11;

Fig. 13 is a plan view of a conductivity modulated MOSFET according to a sixth embodiment of the present invention;

Fig. 14 is a sectional view of the MOSFET taken along the line XIV - XIV of Fig. 13;

Fig. 15 is a plan view showing a modification of the conductivity modulated MOSFET of Fig. 14;

Fig. 16 is a sectional view of the MOSFET taken along the line XVI - XVI of Fig. 15;

Fig. 17 is a plan view of a conductivity modulated MOSFET according to a seventh embodiment of the present invention;

Fig. 18 is a sectional view of the MOSFET taken along the line XVIII - XVIII of Fig. 17;

Fig. 19 is a sectional view of the MOSFET taken along the line IXX - IXX of Fig. 17;

Fig. 20 is a sectional view of the MOSFET taken along the line XX - XX of Fig. 17;

Fig. 21 is a graph showing the latch-up current density JL as a function of the gate width LG;

Fig. 22 is a plan view of a conductivity modulated MOSFET according to an eighth embodiment of the present invention; and

Figs. 23 and 24 are sectional views of conductivity modulated MOSFETs according to ninth and tenth embodiments of the present invention, respectively.

It is very important to increase a current density of a conductivity modulated MOSFET when a parasitic thyristor latches up. For this reason, in a conventional conductivity modulated MOSFET, a great deal of effort has been made to increase this latch-up current density. However, a specific value of the latch-up current density is not proposed. The present inventors experimentally found that the element was not substantially latched up when the latch-up current was larger than the saturation current of the MOSFET in the state that a predetermined gate voltage was applied to set an ON resistance of the conductivity modulated MOSFET to be a sufficiently small value.

That the latch-up current of the MOSFET is larger than the saturation current thereof is defined by th following explanation. A MOSFET is directly connected to a 100-V constant voltage source at a temperature of 25°C. A gate voltage VG is increased from 0 V to $10^2 \cdot d$ (V) (where d is the thickness (μm) of the gate oxide film) within 200 nsec, and a current flows through the MOSFET for 10 μsec to obtain a forward voltage drop of about 100 V. Thereafter, when the gate voltage is set at 0 V or less within 200 nsec, the MOSFET is not latched up but turned off, thus defining the fact that the latch-up current is larger than the saturation current. It should be noted that a resistor of 10-Ω or more cannot be inserted between the gate and the gate terminal of the MOSFET in order to increase the gate voltage from 0 V to $10^2 \cdot d$ (V) within 200 nsec. A latch-up current value described hereinafter is measured including resistance load when the gate voltage is decreased from a predetermined value VG to 0 V or less within 200 nsec as the above description. This latch-up current value is different from that of M.F. Chang et al, which is obtained by inserting a resistance between a gate circuit and an element of between the gate and source terminals.

A conductivity modulated MOSFET according to a first embodiment of the present invention will be described with reference to Figs. 1 to 3.

A high-resistance n^--type layer 12 having an impurity concentration of 2×10^{14})cm^3 is epitaxially grown on a p^+-type Si substrate 10. Several p^+-type guard ring layers 14 are formed to surround an effective element region so as to assure a high withstand voltage. At the same time, a deep (about 10 μm) p^+-type layer 16 serving as part of the base diffusion layer is formed. Thereafter, a gate oxide film 18 is formed to a thickness of 1,000 Å, and then a gate electrode 20 of a polycrystalline silicon film having a thickness of 5,000 Å is formed on the gate oxide film 18. A p-type base diffusion layer 22 is formed using the gate electrode 20 as a mask. A shallow p^+-type layer 24 is formed in the layer 22. An n^+-type source diffusion layer 26 is formed by high concentration and shallow ion implantation of As (arsenic) using the electrode 20 as a mask. a channel region 28 is formed under the gate electrode 20, and thereafter a CVD-SiO_2 film is formed to cover the entire surface. A contact hole is formed in this CVD-SiO_2 film, and a source electrode 30 is formed within the contact hole. A drain electrode 32 is formed on the lower surface of the substrate 10. The p-type base diffusion layer 22 has a depth of 7 μm, and the source diffusion layer 26 has a depth of 0.2 μm. A width LG of a portion of the gate electrode 20 immediately on the high-resistance n^--type layer 12 is 30 μm, and a width LS of the source region is 45 μm. The source comprises a strip shape, as shown in Fig. 1.

The process for deriving the mathematical expressions for the design parameters in this embodiment will be described. A current for latching up the conductivity modulated MOSFET is first obtained. When the widths LS and LG (Figs. 1 and 2) of the source region and the gate electrode are sufficiently small, a substantially uniform hole current flows through an element. The total current density is given as J. When the parasitic thyristor is latched up, the current density is given as JL. In addition, wh n the area (the area of the portion under which the high-resistance semiconductor layer 12 is immediately formed) of the gate electrode 20 within unit area (1 cm^2) of the effective element region is given as SG, a current I flowing into the high-resistance semiconductor layer 12 under the portion of the gate electrode 20 within the unit area is given as follows:

$I = SG \cdot JL$ ...(1)

When the overall peripheral length of all the p-type base diffusion layers 22 and 16 which contacts the high-resistance semiconductor layer 12 per unit area of the element area is given as T, the hole current of the total current given by equation (1) finally flows into the layer 22 in the arrow direction indicated in Fig. 2. Therefore, a current Ib flowing per unit peripheral length of p-type base diffusion layer 22 is defined below:

$Ib = SG \cdot JL \cdot \alpha P/T$ ...(2)

where αP is the ratio of the hole current to the total current. When an average resistance from the unit peripheral length of the base diffusion layer 22 to the source electrode 30 is given as Rb, a voltage drop by the current Ib in the base diffusion layer 22 is:

$V = Rb \cdot SG \cdot JL \cdot \alpha P/T$ ...(3)

When the voltage V exceeds a built-in voltage Vbi at the junction of the source and the base, the parasitic thyristor is latched up. Substitution of Vbi into V in equation (3) yields equation (4) below:

$JL = Vbi \cdot T/(Rb \cdot SG)$ ...(4)

Since the channel disappears in the transient state during switching and the entire current is regarded as the hole current, condition $\alpha P = 1$ is established in equation (4).

When a current flowing per unit area in the saturation region is given as JS, JS is expressed from the MOSFET theory as follows,

$JS = (W/2l)\mu Ci(VG - VT)^2/(1 - \alpha P)$ ...(5)

where

W: the channel width per unit area
l: the channel length
μ: the electron mobility
Ci: the gate capacitance per unit area, and
VT: the threshold voltage.

When the current JL is larger than the current JS, the parasitic thyristor will not be latched up in principle. Therefore,

$Vbi \cdot T/(Rb \cdot SG) > (W/2l)\mu Ci(VG - VT)^2/(1 - \alpha P)$ ...(6)

When the dielectric constant of the gate insulating film 18 is ε and its thickness is d, equation (6) can be rewritten as follows since condition $Ci = \varepsilon/d$ is established:

$W \cdot SG/(T \cdot l \cdot d) < 2Vbi(1 - \alpha P)Rb \cdot \mu \cdot \varepsilon(VG - VT)^2$ ...(7)

The values in the right-hand side of equation (7) are constant except for VG and Rb since αp is sufficiently smaller than 1. The voltage VG is set at about 15 V which can normally drive an IC. A minimum attainable voltage Rb is limited in practice. Therefore, the value given by the right-hand side of equation (7) can be regarded as a constant. When this constant is given as AM,

$W \cdot SG/(T \cdot l \cdot d) < AM$ ...(8)

When equation (8) is satisfied, a maximum current at a gate voltage of 15 V will not latch up the parasitic thyristor. Therefore, this conductivity modulated MOSFET will not be latched up and be turned off in principle.

However, in practice, when a voltage drop of 100 V or more across the element is produced or an excessive current flows therethrough, the element temperature is increased to break down the element. Even in this case if the left-hand side of equation (8) is sufficiently small, breakdown will not easily occur. This will be described with reference to data of Fig. 3.

Referring to Fig. 3, it will be explained that, at the point of VSC (a voltage applied to the element) = 300 V along the ordinate, the element will not be broken down even if a current flows in the element for 10 μs after the element is connected to a 300-V constant voltage source at the gate voltage VG = 15 V and case temperature = 25°C. Of course, a voltage drop of the element in this case is the same 300 V as a 300 V voltage source. A voltage source up to a 300-V source can be used for a 600-V element. When the voltage VSC exceeds 300 V, the element will not be broken down at least for 10 μs even if the power source voltage is directly applied to a system using this element upon short-circuiting of an external load. The breakdown of the element will be prevented if the element is turned off during the 10 μs. Referring to Fig. 3, in order not to break the element down even if a current flows for 10 μs at a voltage of 300 V while the gate voltage VG is set at 15 V, the following condition must be satisfied:

$W \cdot SG/T \cdot l \cdot d) < 1.1 \times 108$... (9)

The value given by the above condition is a non-dimensional parameter.

In the conductivity modulated MOSFET according to the first embodiment shown in Figs. 1 and 2, SG = 30/(30 + 45) = 0.4 (cm^2), and the length T of the p-type base diffusion layer is substantially equal to the channel width W. In addition, since the channel length l is about 5.5 μm, the following results are obtained

$W \cdot SG/(T \cdot l \cdot d) = SG/(l \cdot d)$
$= 7.3 \times 10^7$

In the above embodiment, when a voltage of 500 V is applied between the drain and the source while a voltage of 15 V is applied to the gate, a current of 300 A/cm^2 flows through the element. In this case, the element will not be broken down for 10 μs. The element has a static breakdown voltage of 600 V and is normally used at a power source voltage of 300 V or less. Therefore, since the element is not broken down at the power source voltage of 500 V in the above embodiment, the electrical characteristics of the element can be regarded to be sufficient.

Similarly, in an element having a static breakdown voltage of 1,200 V, the voltage VSC is set to be 600 V.

Fig. 4 shows a diffusion layer pattern according to a second embodiment. The pattern of the second embodiment is substantially the same as that of the first embodiment except that a p-type base diffusion 22 comprises a plurality of island regions, and the manufacturing process of the second embodiment is the same as that of the first embodiment. The same reference numerals as in the second embodiment denote the same parts as in the first embodiment. In the second embodiment, four corners of an n^+-type source region 26 are omitted so as not to entirely cover the peripheral portion of a p-type base diffusion layer 22. The length T of the layer 22 differs from the width W to obtain a ratio W/T = 0.8. In addition, conditions LG = 20μ and LS = 45 μm are given. Therefore,

$W \cdot SG/(T \cdot l \cdot d) = 7.6 \times 10^7$

Substantially the same characteristics as in the first embodiment can be obtained in the second embodiment.

In the above embodiment, the gate voltage is set at 15 V. However, when the ambient temperature of the lement is kept at 25°C, the gate voltage may be 10 V to set the latch-up current to b larger than the saturation current if condition (10) below is satisfied:

$$W \cdot SG/T \cdot l \cdot d) < 1.46 \times 10^8 \quad \ldots (10)$$

In the conductivity modulated MOSFET satisfying condition (10), when heavy metal diffusion or electron beam irradiation is performed in the high-resistance n-type semiconductor layer 12, i.e., when a lifetime killer is injected therein to shorten the carrier lifetime, the saturation current can be set small. In this case, even if a temperature rise occurs, the latch-up phenomenon of the MOSFET can be prevented.

A conductivity modulated MOSFET according to a third embodiment of the present invention will be described with reference to Figs. 5 and 6.

According to the third embodiment, a base stripe layer is formed in the substrate. A method of fabricating the above MOSFET will be described with reference to the steps thereof. A p^+-type Si substrate 10 is prepared. An n^--type layer 12 having a low impurity condentration and a resistivity of 50 Ωcm or more is epitacially formed to a thickness of about 100 μm on the substrate 10. The surface of layer 12 is oxidized to form a gate oxide film 18. A gate electrode 20 of a polycrystalline silicon film having a thickness of 5,000 Å is formed on the gate oxide film 18. Thereafter, boron is implanted using the gate electrode 20 as a mask and is diffused to a depth of 8 μm to form a p-type base layer 22. An oxide pattern (not shown) having a hole for forming the source layer is formed in a window surrounded by the gate electrode 20, and As ions are implanted at a dose of $5 \times 10^{15}/cm^2$ using the oxide pattern and the electrode 20 as masks. The resultant structure is annealed to form an n^+-type source layer 26a. As is apparent from Fig. 5, the source layer 26a comprises a plurality of discrete island regions. Thereafter, a high-impurity p^+-type layer 24 is formed in the layer 22, and a source electrode 30 is formed to contact the p^+-type layer 24 and the n^+-type source layer 26a. A drain electrode 32 is formed by deposition of V-Ni-Au on the lower surface of the substrate 10. A channel region 28 alternately comprises effective channel portions 28a subjected to normal MOSFET operation and portions 40 which are not subjected to MOSFET operation since the source layer is not present.

In the MOSFET in this embodiment, when the element is turned on, among the hole current components injected from the n^--type layer 12 open under the gate electrode 20 to the p-type base layer 22, components flowing through the portions 40 do not flow under the source layer 26a but directly flow into the source electrod 30. Therefore, as compared with the conventional structure, the lateral resistance under the source layer can be effectively decreased, and the latch-up phenomenon does not occur up to a large current.

In the above embodiment, when the conductivity modulated MOSFET is designed to satisfy equations (9) or (10), the latch-up phenomenon can be further prevented.

Referring to Figs. 5 and 6, a plurality of n^+-type source layers 26a are independent of each other. However, as shown in Fig. 7, n^+-type source layers 26 may be commonly connected through a small width region. In this case, when the width of the source layers at channel portions 42 is substantially small, the same effect as in the above embodiment can be expected.

A conductivity modulated MOSFET according to a fourth embodiment of the present invention will be described with reference to Figs. 8 and 9. The same reference numerals as in the fourth embodiment denote the same parts as in the previous embodiments, and a detailed description thereof will be omitted. According to the fourth embodiment, a p^+-type layer 24 obtained by diffusion in a p-type base layer 22 has an indented edge pattern, i.e., the edges terminated at a channel region 28 and the edges terminated under source layers 26 are alternately formed. In other words, the channel region 28 alternately comprises portions 44 with p^+-type layers 24 and portions 28a without p^+-type layers 24. The n^+-type source layers 26 are continuously formed at two sides within the p-type base layer 22 in the same manner as in the conventional structure.

In this embodiment, the channel portions 44 have a higher threshold value than that of the channel portions 28a. In other words, the threshold value of the element is determined by the channel portion 28a. More particularly, when an ON gate signal is supplied to a gate electrode 20, the channel portion 28a is turned on upon MOSFET operation, while the channel portion 44 is kept off. In the ON state wherein conductivity modulation is occurred in the N_--type layer 12 and an excessive current flows, a hole current from the n_--type layer 12 also flows in the channel portion 44. Since the p^+-type layer 24 is formed entirely under the source layer 26 in the channel portion 44, a lateral resistance under the sourc layer 26 is small as compared with that under the channel portion 28a. Therefore, a voltage drop caused by a current flowing through the channel portion 44 is small. As a result, the latch-up phenomenon does not occur even if an excessive current flows in this embodiment.

In the embodiment shown in Fig. 8, the n^+-type source layers 26 are continuously formed at two side of the p^+-type base layer 22. However, when the layers 26 are replaced with discrete layers 26a on portion 28a in the same manner as in Fig. 5, i.e., when the embodiment of Fig. 5 is combined with that of Fig. 8, a further effect can be obtained. Its plan view is shown in Fig. 10. Therefore, a conductivity modulated MOSFET which is free from the latch-up phenomenon up to a current density of $1,500\ A/cm^2$ can be obtained.

A conductivity modulated MOSFET according to a fifth embodiment of the present invention will be described with reference to Figs. 11 and 12. According to this embodiment, n^+-type sourc layers 26 are continuously formed at one side of a p-type base layer 22 and are not formed at the other side thereof. In this case, in the channel region 28, only channel portions 28a located at the source layer 26 are subjected to MOSFET operation, but channel portions 40 ar not

subjected to MOSFET operation. In the same manner as the previous embodiments, among the current components injected from the n^--type layer 12 to the p-type base layer 22, components passing through channel portions 40 directly flow into the source electrode 30 without flowing under the source layer 26, thereby effectively preventing the latch-up phenomenon.

In the above embodiment, the first conductivity type comprises p type, and the second conductivity type comprises n type. However, these conductivity types may be reversed to obtain the same effect as in the previous embodiments. In addition, the n^--type layer 12 may serve as a starting substrate, and the p^+-type drain 10 may be formed by diffusion.

In the fourth and fifth embodiments, if conductivity modulation MOSFETs are fabricated to satisfy equations (9) or (10), a latch-up phenomenon can further be prevented.

A conductivity modulated MOSFET according to a sixth embodiment of the present invention will be described with reference to Figs. 13 and 14. The same reference numerals as in the third embodiment denote the same parts in the sixth embodiment.

The fabrication steps of the MOSFET will be described. A p^+-type Si substrate 10 is prepared. An n^--type layer 12 having a low impurity concentration and a resistivity of 50 Ωm is epitaxially gown on the substrate 10 to a thickness of 100 µm. The surface of the layer 12 is oxidized to form a gate oxide film 18, and a gate electrode 20 of polysilicon having a thickness of 5,000 Å is formed on the film 18. Thereafter, boron is diffused to a depth of 4 µm, using the gate electrode 20 as a mask, to form p-type base layers 22a and 22b. An oxide pattern (not shown) having openings for forming the source layers is formed within windows formed by the gate electrode 20, and As ions are implanted using the oxide pattern and the gate electrode 20 as masks at a dose of $5 \times 10^{15}/cm^2$ to form the source layers. The resultant structure is annealed to form n^+-type source layers 26. As is apparent from Fig. 14, the layers 26 are not formed in the base layers 22b. Thereafter, p^+-type layers 24a and 24b are formed by diffusion in the p-type base layers 22a and 22b. Source electrodes 30a and 30b are formed to contact the layers 24a, 24b and 26. A drain electrode 32 is formed by depostion of V-Ni-Au on the lower surface of the substrate 10. A channel region 28 has effective channel portions 28a subjected to normal MOSFET operation and portions 40 which are not subjected to MOSFET operation in a given order.

In the MOSFET of this embodiment, among the hole current components injected from the n^--type layer 12 existing under the gate electrode 20 to the p-type base layers 22a, 22b, the components passing through the channel portions 40 directly flow into the source electrode 30b without flowing under the source layers 26. Since an amount of hole current along the lateral direction under the source layers is decreased as compared with the conventional structure, the latch-up phenomenon does not occur even if an excessive current flows therethrough.

In the above embodiment, the layers 26, 24a and 24b comprise island regions. However, as shown in Figs. 15 and 16, island regions may be replaced with the stripe regions. Other arrangements of Figs. 15 and 16 are the same as those of Figs. 15 and 16 denote the same parts as in Figs. 13 and 14, and a detailed description thereof will be omitted.

When the conductivity modulated MOSFETs are formed to satisfy equations (9) or (10) in the sixth embodiment, the latch-up phenomenon is further prevented.

A conductivity modulated MOSFET according to a seventh embodiment of the present invention will be described with reference to Figs. 17 to 20.

An n^--type high-resistance layer 112 is formed on a p^+-type drain layer 110. P and p^+-type base diffusion layers 122 and 116 are formed on the layer 112. An n^+-type source diffusion layer 126 is formed in the layer 122. A gate electrode 120 (dotted region) of a polycrystalline silicon film is formed on a gate insulating film 118 which is provided on a channel region 128. The channel region 128 is provided in an exposed portion of the wafer between the layers 126 and 112. A source electrode 130 is formed to contact the layers 126 and 122. A drain electrode 132 is formed on the layer 110 as the lower surface of the wafer.

The first feature of this embodiment lies in the fact that the high-resistance layers 112 under the gate electrodes 120 are formed to be rectangular and arranged in a matrix form, and channel regions 128 are arranged along the long sides of the rectangular layers 112. The reason why the layer 112 has a rectangular shape is that the width of the channel region 128 can be maximized in the rectangular island shape if the layer 112 is formed in an island fashion. The second feature lies in the fact that the rectangular portions of the layer 112 are completely surrounded by the layers 122 and 116 to constituted island portions. In other words, the gate electrode 120 is continuously formed on the surface of the substrate so as to cover the channel region 128 and the rectangular portions. Al stripe gate electrodes 150 are formed at positions where the source electrodes 130 are not present. As shown in Figs. 18 to 20, a p^+-type base diffusion layer 116 is formed under the source electrode 130 and the Al electrode 150 formed on the gate electrode 120. The rectangular portion of the high-resistance layer 112 is formed to be surrounded by the base diffusion layers 122 and 116.

In practice, the p^+-type Si substrate (to be the drain layer 110) serves as the starting substrate. The layer 112 is epitaxially grown, and the resultant bulk substrate is used to sequentially perform impurity diffusion and electrode formation. However, the layer 112 may be used as a starting substrate.

As is apparent from Fig. 17, the overall width of the channel region 128 formed around the layer 112 existing under the gate electrode 120 is substantially the same as the peripheral length of the opening of the p^+-type base diffusion layer 116 which contacts to the source electrode 130. For this reason, the spreading resistance caused by a difference between the lengths of the layer 116 and the channel region 128 is eliminated, and a base diffusion layer resistance under the source layer 126 can be small.

Only the gate electrode 120 of a polycrystalline silicon film is formed on the rectangular portion of the

layer 112. In other words, no Al electrode 150 is formed thereon, so that the gate electrode width LG at this portion can be sufficiently small. The width LG is inversely proportional to the latch-up current density.

The fact that the drain current is inversely proportional to the width LG upon latching of the parasitic thyristor can be demonstrated, as in the equation (4), as follows. A substantially uniform current flows under the gate insulating film 118 and then into the p-type base layer 128, so that the following current IP flows per unit width of the channel region 128 under the gate insulating film 118:

$$IP = SG \cdot JP/T \quad \ldots (11)$$

where

JP: the hole current density

SG: the area of the gate electrode on the rectangular portion of the n^--type high-resistance layer per unit area and

T: the peripheral length of the p-type base diffusion layer per unit area including p^+-base diffusion.

The current IP flows into the base diffusion layer under the source diffusion layer. When a voltage drop caused by the resistance Rb under the source diffusion layer exceeds the built-in voltage Vbi between the base and the source, the parasitic thyristor is turned on. This condition is given as follows:

$$Vbi = IP \cdot Rb = SG \cdot JP \cdot Rb/T \quad \ldots (12)$$

where

Rb the resistance from the channel region per unit peripheral length to the p^+-type contact.

When the above equation is solved for JP,

$$JP = Vbi \cdot T/SG \cdot Rb \quad \ldots (13)$$

The inversion layer of the channel disappears when the element is turned off. The total current comprises the hole current, so that the latch-up current density JL is JP/αP, where αP is the ratio of the hole current to the total current. As mentioned above, αP = 1, so that JL is given as follows:

$$JL = Vbi \cdot T/SG \cdot Rb \quad \ldots (14)$$

SG/T is substantially LG, so that JL is inversely proportional to LG. This result is apparent from the experimental data (Fig. 21) obtained by the present inventors.

In a sample MOSFET, LG = 20 μm is given. According to this embodiment, a latch-up current density of 750 A/cm^2 is obtained to effectively prevent the latch-up phenomenon. When the entire operating area was given as 20 mm^2, the turn-off operation up to a current of 150 A could be performed.

The present invention is not limited to the particular embodiments described above. For example, the shape of the layer 112 exposed on the surface of the wafer need not be a rectangular shape. As shown in Fig. 22, the layer 112 may have a hexagonal shape. In this embodiment, a channel region 128 is formed to surround a hexagonal high-resistance layer 112. The same referenc numerals as in Fig. 22 denote the same parts as in Fig. 17. Assum that a width of a source diffusion layer 126 is given as Ln and that a sum (i.e., peripheral length) of the widths of the channel region 128 is given as T (= W). A path of the hole current flowing from the layer 112 to p and p^+-type layers 122 and 116 through a portion under the channel region 128 comprises a radial path spreading from the center to the outer direction. The base resistance Rb under the source layer is smaller than that in the case wherein the current path is directed from the outer side to the inner side, if T in the former is equal to that in the latter.

In equation (14), SG is the area of the rectangular portion of the layer 112 and T is the peripheral length of the rectangular portion (i.e., the width of the channel). A product SG·Rb of MOSFET having the current path directed from the inner to outer sides can be decreased, as compared with the MOSFET having the current path directed from the outer to the inner sides if T in the former is equal to that in the latter. Therefore, the latch-up current density JL can be increased.

The island high-resistance layer may resemble a rectangle having at least two parallel side wherein the channel regions are formed along the four sides or two long sides.

In the embodiment described above, the drain electrode is formed on a surface opposite to that having the source and gate electrodes. In other words, a vertical MOSFET is exemplified. However, the present invention can also be applied to a lateral MOSFET, as shown in Fig. 23. Fig. 23 is a sectional view showing the main part of a lateral MOSFET. An n^--type high-resistance layer 212 is formed on a p^+-type layer 210. A p-type base diffusion layer 222 and an n^+-type source diffusion layer 226 are formed in the surface of the layer 212. A gate electrode 220 is formed on a gate insulating film 218 which is formed on a channel region 228 between the layers 226 and 212. A source electrode 230 is formed to contact the layers 226 and 222. The basic structure of this MOSFET is the same as that of each of the above embodiments. In addition, according to this embodiment, an n-type layer 260 is formed in the surface of the n^--type layer 212, and a p^+-type drain layer 262 is formed in the layer 260. A drain electrode 232 is formed on the drain layer 262. The layer 260 prevents extension of a depletion layer produced when the conductivity modulated MOSFET is operated in a forward blocking region, thereby decreasing the width LDs of the window of the layer 212. The p-type base diffusion layer 222 may completely surround the window of the layer 212 to obtain the same effect as in the previous embodiments. The entire remaining embodiments according to this invention may be applied to the above lateral element.

As shown in Fig. 24, the p^+-type layer 210 of Fig. 23 may be replaced with a n^+-type layer 264.

In the embodiments after the seventh embodiment, if conductivity modulated MOSFETs are prepared to satisfy equations (9) or (10), the latch-up phenomenon can be further prevented.

In the entire embodiments, the n^--type high-resistance layer may be used as a starting substrate to form the other semiconductor layers.

CLAIMS

1. A conductivity modulated metal oxide semiconductor field effect transistor, comprising:

a semiconductor substrate of a first conductivity type which has first and second surfaces;

a high resistance semiconductor layer of a second conductivity type which is formed on said first surface

of said semiconductor substrate and has a high resistance, said high resistance semiconductor layer being provided with a third surface contacting said first surface and a fourth surface opposite to said third surface;

a base layer of the first conductivity type which is formed in said fourth surface of said high resistance semiconductor layer;

a source layer of the second conductivity type which is formed in said base layer;

a gate electrode formed on a gate insulating film which is formed on a channel region, said channel region being formed in a surface of said base layer between said fourth surface of said high resistance semiconductor layer and said source layer;

a source electrode ohmic-contacting layer and said base layer; and

a drain electrode formed on said second surface of said semiconductor substrate,

wherein the improvement comprises

said conductivity modulated metal oxide semiconductor field effect transistor having a saturation current smaller than a latch-up current when a predetermined gate voltage is applied to said gate electrode.

2. The transistor according to claim 1, wherein portions which are not or can hardly be subjected to metal oxide semiconductor field effect transistor operation are cyclically formed between said source electrode and said fourth surface of said high resistance semiconductor layer.

3. The transistor according to claim 2, wherein said portion which is not subjected to metal oxide semiconductor field effect transistor operation comprises a portion without said source layer along a direction of a width of a channel, thereby forming a hole current path along which carriers flow from a drain side to said source electrode without passing under said source layer.

4. The transistor according to claim 2, wherein the portion which can hardly be subjected to metal oxide semiconductor field effect transistor operation has a channel region having a higher threshold value than that of other regions.

5. The transistor according to claim 1, wherein said fourth surface of said high resistance semiconductor layer is surrounded by said base layer to constitute an island region.

6. The transistor according to claim 5, wherein said fourth surface of said high resistance semiconductor layer has a rectangular shape.

7. The transistor according to claim 5, wherein said gate electrode comprises a polycrystalline silicon film formed to cover said island region and a metal film formed on said polycrystalline silicon film, said base layer of the first conductivity type being formed under said metal film to isolate said island region.

8. The transistor according to claim 1, wherein when an overall channel width per unit area (1 cm^2) of an effective element region is W (μm), an area of a portion of said gate lectrode which is formed immediately on said high resistanc semiconductor layer within said unit area is SG (μm^2), an overall peripheral length of said base layer within said unit area is T (μm), a channel length is l (μm) and a thickness of said gate insulating folm is d (μm), condition $(W \cdot SG)/(T \cdot l \cdot d) < 1.46 \times 10^8$ is satisfied.

9. The transistor according to claim 8, wherein portions which are not or can hardly be subjected to metal oxide semiconductor field effect transistor operator are cyclically formed between said source electrode and said fourth surface of said high resistance semiconductor layer.

10. The transistor according to claim 9, wherein said portion which is not subjected to metal oxide semiconductor field effect transistor operation comprises a portion without said source layer along a direction of a width of a channel, thereby forming a hole current path along which carriers flow from a drain side to said source electrode without passing under said source layer.

11. The transistor according to claim 9, wherein the portion which can hardly be subjected to metal oxide semiconductor field effect transistor operation has a channel region having a higher threshold value than that of other regions.

12. The transistor according to claim 8, wherein said fourth surface of said high resistance semiconductor layer is surrounded by said base layer to constitute an island region.

13. The transistor according to claim 12, wherein said fourth surface of said high resistance semiconductor layer has a rectangular shape.

14. The transistor according to claim 12, wherein said gate electrode comprises a polycrystalline silicon film formed to cover said island region and a metal film formed on said polycrystalline silicon film, said base layer of the first conductivity type being formed under said metal film to isolate said island region.

15. The transistor according to claim 8, wherein a lifetime killer is introduced in said high resistance semiconductor layer to decrease a saturation current of said transistor.

16. The transistor according to claim 15, wherein portions which are not or can hardly be subjected to metal oxide semiconductor field effect transistor operation are cyclically formed between said source electrode and said fourth surface of said high resistance semiconductor layer.

17. The transistor according to claim 16, wherein said portion which is not subjected to metal oxide semiconductor field effect transistor operation comprises a portion without said source layer along a direction of a width of a channel, thereby forming a hole current path along which carriers flow from a drain side to said source electrode without passing under said source layer.

18. The transistor according to claim 16, wherein the portion which can hardly be subjected to metal oxide semiconductor field effect transistor operation has a channel region having a higher threshold value than that of other regions.

19. The transistor according to claim 15, wherein said fourth surface of said high resistance semiconductor layer is surrounded by said base layer to consistute an island region.

20. The transistor according to claim 19, wherein said fourth surface of said high resistance semiconductor layer has a rectangular shape.

21. The transistor according to claim 19, wherein

said gate electrode comprises a polycrystalline silicon film formed to cover said island region and a metal film formed on said polycrystalline silicon film, said base layer of the first conductivity type being formed under said metal film to isolate said island region.

22. The transistor according to claim 1, wherein whan an overall channel width per unit area (1 $cm,^2$) of an effective element region is W (μm), an area of a portion of said gate electrode which is formed immediately on said high resistance semiconductor layer within said unit area is SG (μm^2), an overall peripheral length of said base layer within said unit area is T (μm), a channel length is I (μm) and a thickness of said gate insulating film is d (μm), condition $(W \cdot SG)/(T \cdot I \cdot d) < 1.1 \times 10^8$ is satisfied.

23. The transistor according to claim 22, wherein portions which are not or can hardly be subjected to metal oxide semiconductor field effect transistor operation are cyclically formed between said source electrode and said fourth surface of said high resistance semiconductor layer.

24. The transistor according to claim 23, wherein said portion which is not subjected to metal oxide semiconductor field effect transistor operation comprises a portion without said source layer along a direction of a width of a channel, thereby forming a hole current path along which carriers flow from a drain side to said source electrode without passing under said source layer.

25. The transistor according to claim 23, wherein the portion which can hardly be subjected to metal oxide semiconductor field effect transistor operation has a channel region having a higher threshold value than that of other regions.

26. The transistor according to claim 22, wherein said fourth surface of said high resistance semiconductor layer is surrounded by said base layer to constitute an island region.

27. The transistor according to claim 26, wherein said fourth surface of said high resistance semiconductor layer has a rectangular shape.

28. The transistor according to claim 26, wherein said gate electrode comprises a polycrystalline silicon film formed to cover said island region and a metal film formed on said polycrystalline silicon film, said base layer of the first conductivity type being formed under said metal film to isolate said island region.

29. A conductivity modulated MOSFET, substantially as hereinbefore described with reference to the accompanying drawings.

Printed in the United Kingdom for Her Majesty's Stationery Office, 8818935, 1/86 18996. Published at the Patent Office, 25 Southampton Buildings, London WC2A 1AY, from which copies may be obtained.